Course Title	Digital Logic Design with Verilog HDL
Course Code	EE5334
No. of Credit Hrs (Lecture + Tutorial + Lab)	3 (2+0+1)
No. of Contact Hrs (Lecture + Tutorial + Lab)	4 (2+0+2)
Level-Year	9/10-5
Prerequisite (if any)	EE3301, EE2302

4. Measuring open-circuit voltage & short-circuit current of solar cells
5. Determination of I-V& P-V Characteristics of a Series and Parallel combination of PV Panels / Modules
6. Power Flow calculation of Stand-Alone PV System of DC Load with Battery

5) Teaching Methods:

- Lectures and Discussion
- Videos
- Self-learning
- Laboratory demonstrations

6) Mode of Evaluation: Course Assessment Methods

- Quizzes and assignment
- Major Exams
- Final Exam
- Lab Work

Evaluation

- **Semester Work**
  - Major Exams 30%
  - Quizzes 5%
  - Assignments 5%
  - Lab/Tutorial 20%
- **Final**
  - Paper work 40%

7) Textbook(s):

- Stuart R. Wenham et. al., Applied Photovoltaics, Taylor and Francis, Third edition, 2012.
- R. A. Messenger, Photovoltaic Systems Engineering, CRC Press, fourth edition, 2017.

1) Course Objectives:

This course covers the design, analysis, and debugging of digital electronic circuits using Verilog HDL Language. It includes design methodologies, hierarchical modelling, test and implementation of digital hardware of VLSI Circuits in Verilog HDL.

2) Expected Learning Outcomes:

1. Summarize and explain modern VLSI circuit design methodologies and their implementation. KLO1 [1]
2. Recognize and apply basic Verilog HDL constructs and modeling styles for fundamental digital logic components (e.g., AND, OR, NOT gates). KLO1 [1]
3. Employ and integrate basic logic modules in the design of digital circuits and systems. KLO2 [2]
4. Analyze and design combinational and sequential logic circuits using Verilog HDL. KLO3 [6]
5. Conduct and investigate laboratory experiments on digital logic design techniques using Verilog HDL. KLO3 [6]

3) Course Contents:

1. Overview of Digital Design with Verilog HDL
2. Hierarchical Modeling Concepts
3. Basic Language Concepts
4. Modules and Ports
5. Gate-Level Modeling, Dataflow Modeling and Behavioral Modeling
6. Tasks and Functions
7. Useful Modeling Techniques
8. Timing and Delays
9. Basic Logic Synthesis with Verilog HDL
10. Finite state machines (FSM)

4) Laboratory Experiments

1. Understand the Modelsim/Xilinx-Vivado/Icarus-Verilog (simulator)/any-equivalent tools for design/simulation of digital logic design.
2. Realization of logic gates using Verilog HDL.
3. Realize 8 to 3 Encoder without priority and with Priority using Verilog Code.
4. Implement 4 to 1 Multiplexer and 1 to 4 Demultiplexer on Verilog HDL by a) Gate level modelling b) Data flow modelling.
5. Implementation of 4 to 1 Multiplexer and 1 to 4 Demultiplexer using Behavioral modelling
6. Write a Verilog HDL code to realize 4-bit ALU.
7. Write Verilog HDL Code to realize Flip-Flops.
8. Realization of binary sequence (arbitrary) up down 4-bit counter using the concept of FSM.

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Evaluation

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  - Paper work 40%

7) Textbook(s):

- Samir Palnitkar, Verilog HDL: A guide to Digital Design and Synthesis, 2nd Edition, Prentice Hall, 2003

8) References:

- Z. Navabi, Verilog Digital System, McGraw Hill, 2nd Edition, 2005